CLAIMS

I CLAIM:

1. A phase-locked loop, comprising:

a phase detector receiving an input signal and a first internal periodic signal and providing a phase signal indicative of a phase difference between said input signal and said internal signal;

a rotator receiving said phase signal and providing a first and a second periodic signal each having a period being a function of said phase difference, said first and said second periodic signal being 90 degrees out of phase; and

an interpolator circuit linearly combining said first and second periodic signals with a third and a fourth periodic signal to provide said first internal periodic signal.

2. A phase-locked loop as in Claim 1, wherein said interpolator circuit further providing a second internal periodic signal, said second internal periodic signal being 90 degrees out of phase relative to said first internal periodic signal.

3. A phase-locked loop as in Claim 1, further comprising a low-pass filter provided between said phase detector and said rotator.

4. A phase-locked loop as in Claim 2 wherein said rotator comprises an integrator.

5. A phase-locked loop as in Claim 1, wherein said first (Q) and second (I) periodic signals are given by the equations:

$$Q = A\cos(kf(p))$$

$$I = A\sin(kf(p))$$

where A is an amplitude of each of signals Q and I, k is a gain of said rotator circuit, and $f(p)$ represents a function of said phase difference.

6. A phase-locked loop as in Claim 5, wherein said phase difference is represented in said phase signal as a voltage.

7. A phase-locked loop as in Claim 5, wherein said function comprises integration.

8. A phase-locked loop as in Claim 1, wherein said third and fourth periodic signals each have a frequency being substantially a frequency of said input signal.

9. A phase-locked loop as in Claim 5, said rotator further comprising an enforcer providing an error signal indicating a deviation in said first and second periodic signals from said equations.

10. A phase-locked loop as in Claim 9, wherein said error signal is a function of the value $\Delta = r^2 - I^2 - Q^2$, where r is an amplitude of each of signals I and Q.

11. A phase-locked loop as in Claim 5 wherein said third (x) and fourth (y) periodic signals are given by the equations:

$$x = \sin\omega t\,,$$

$$y = \cos\omega t\,,$$

where ω represents a frequency of said third and fourth periodic signals.

12. A phase-locked loop as in Claim 11, wherein said first internal periodic signal $S(t)$ is given by:

$$S(t) = \sin(\omega t - \varphi) ,$$

where φ is indicative of said phase difference.

13. A method for providing a phase-locked loop, comprising:

receiving an input signal and a first internal periodic signal and providing a phase signal indicative of a phase difference between said input signal and said internal signal;

receiving said phase signal and providing a first and a second periodic signal each having a period being a function of said phase difference, said first and said second periodic signal being 90 degrees out of phase; and

linearly combining said first and second periodic signals with a third and a fourth periodic signal to provide said first internal periodic signal.

14. A method for providing a phase-locked loop as in Claim 13, further providing a second internal periodic signal, said second internal periodic signal being 90 degrees out of phase relative to said first internal periodic signal.

15. A method for providing a phase-locked loop as in Claim 1, further comprising providing a low-pass filter between said phase detector and said rotator.

16. A method for providing a phase-locked loop as in Claim 2 wherein said rotator comprises an integrator.

17. A method for providing a phase-locked loop as in Claim 1, wherein said first (Q) and second (I) periodic signals are given by the equations:

$$Q = A\cos(kf(p))$$

$$I = A\sin(kf(p))$$

where A is an amplitude of each of signals Q and I, k is a gain of said rotator circuit, and $f(p)$ represents a function of said phase difference.

18. A method for providing a phase-locked loop as in Claim 17, wherein said phase difference is represented in said phase signal as a voltage.

19. A method for providing a phase-locked loop as in Claim 5, wherein said function comprises integration.

20. A method for providing a phase-locked loop as in Claim 12, wherein said third and fourth periodic signals each have a frequency being substantially a frequency of said input signal.

21. A method for providing a phase-locked loop as in Claim 17, further comprising providing an error signal indicating a deviation in said first and second periodic signals from said equations.

22. A method for providing a phase-locked loop as in Claim 17, wherein said error signal is a function of the value $\Delta = r^2 - I^2 - Q^2$, where r is an amplitude of each of signals I and Q.

23. A method for providing a phase-locked loop as in Claim 17 wherein said third (x) and fourth (y) periodic signals are given by the equations:

$$x = \sin\omega t\ ,$$

$$y = \cos\omega t\ ,$$

where ω represents a frequency of said third and fourth periodic signals.

24. A method for providing a phase-locked loop as in Claim 23, wherein said first internal periodic signal $S(t)$ is given by:

$$S(t) = \sin(\omega t - \varphi) ,$$

where φ is indicative of said phase difference.